Camera Interface to HDZero™ VTX

This document defines the interface between Camera and VTX of HDZero™. It answers the following questions:

1. What is the interface between a HDZero™ compatible Camera and HDZero™ VTX?
2. How to put encryption IC on Camera?
3. How CAM_CFG is generated?

1. Camera Interface with VTX

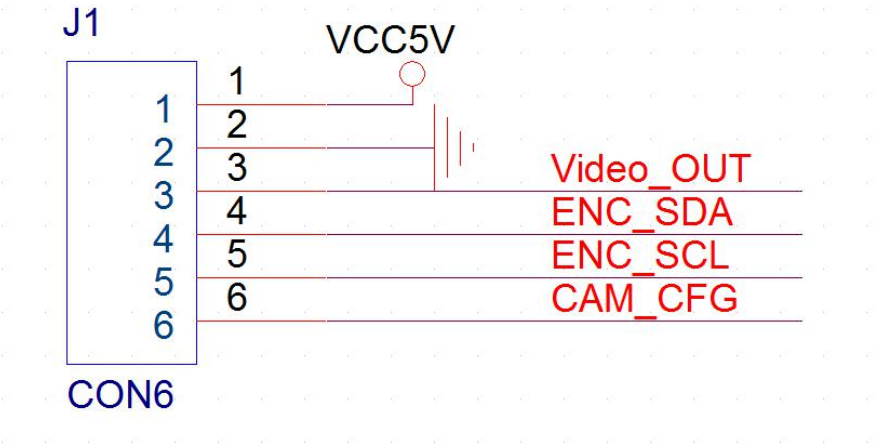


FIG 1. J1 definition

J1 defines the interface between Camera and VTX.

Pin No	Pin Name	Definition
1	VCC5V	It is powered from VTX to Camera. 5 Volts,
2	GND	Ground
3	Video Out	Analog HD Composite Video (TVI-50 or TVI-60)
4	ENC_SDA	Dedicated pin to encryption IC
5	ENC_SCL	Dedicated pin to encryption IC
6	CAM_CFG	Analog level signal for camera setting

2. About encryption IC

Each HDZero™ compatible Camera has to integrate an encryption IC for authentication. The encryption IC is available from Divimath,Inc. For more information, please contact info@divimath.com.

FIG 2 shows the schematic how to integrate the IC into camera: U1 is the encryption IC, and ENC_SCL and ENC_SDA are connected from J1 directly.

FIG 3 shows the detailed packaging information.

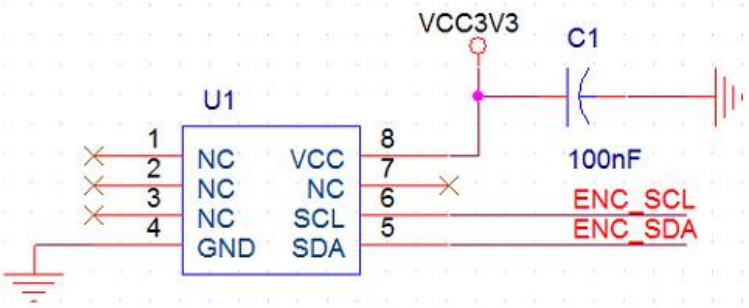
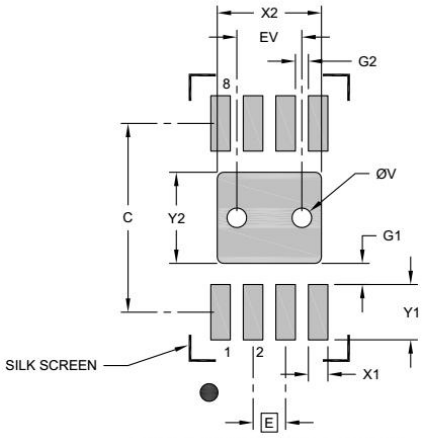


FIG 2. Encryption IC circuit

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy YNZ Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.33		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during

FIG 3. Encryption IC package

3. About CAM_CFG signal

CAM_CFG signal is a signal to camera from a parameter board (left board of FIG 4) via VTX board (right board of FIG 4). CAM_CFG is aliased as OSD for major analog cameras.

FIG 5 shows the schematic how CAM_CFG is generated.

FIG 4. A parameter board connecting with VTX

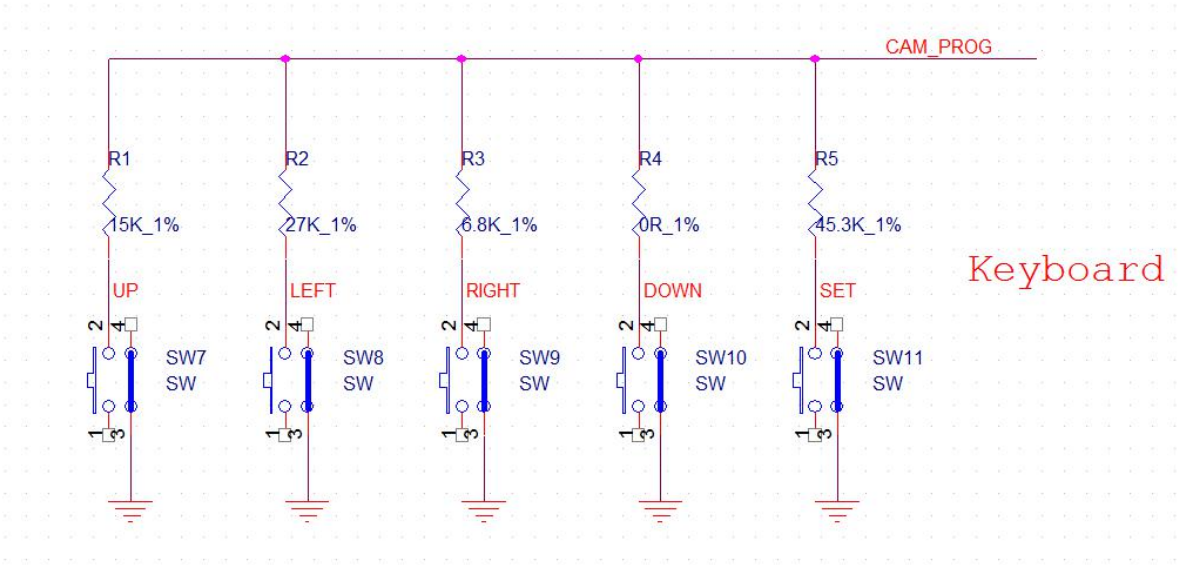


FIG 5. Schematic of how CAM_CFG is generated